WHAT IS CLAIMED IS:

1. A high code-density microcontroller architecture with changeable instruction formats, comprising:

a memory for storing compressed instructions each having a group prefix followed by at least one index;

a compressed instruction buffer for storing and buffering the instructions fetched from the memory;

a next address logic for accessing an instruction from the memory or sending out a next instruction in the compressed instruction buffer directly; and

an instruction decompressor for decompressing the compressed instruction sent from the compressed instruction buffer into an original instruction,

wherein the instruction decompressor has a plurality of instruction group decoding tables, each being stored with the original instructions of a predetermined type, and the instruction decompressor selects one of the instruction group decoding tables based on the group prefix of the compressed instruction for searching a corresponding original instruction therein by the index of the compressed instruction.

2. The architecture as claimed in claim 1, further comprising a decoding and execution unit including a control signal decoder for decoding the original instructions into control signals and an execution core controlled by the control signal decoder for performing corresponding processes.

3. The architecture as claimed in claim 1, wherein the instruction

decompressor further includes a multiplexer and instruction group extractor for extracting the compressed instruction sent from the compressed instruction buffer, controlling the multiplexer to select one of the instruction group decoding tables based on the group prefix of the compressed instruction, and searching the corresponding original instruction therein by the index of the compressed instruction for being outputted by the multiplexer to the decoding and execution unit to be executed.

4. The architecture as claimed in claim 1, wherein the memory is a read-only memory (ROM).

5. The architecture as claimed in claim 1, wherein the compressed instruction in the memory consists of a first group prefix followed by an instruction index for searching a first instruction group decoding table stored with the corresponding original instructions.

6. The architecture as claimed in claim 1, wherein the compressed instruction in the memory consists of a second group prefix followed by an op-code index representing a branch condition code, and a displacement index representing a branch target address; the op-code and the displacement indices are used to search a second instruction group decoding table including a first sub-table and a second sub-table, respectively, the first sub-table being stored with the branch condition codes of the corresponding original instructions, the second sub-table being stored with the branch target addresses of the corresponding original instructions.

7. The architecture as claimed in claim 1, wherein the compressed

instruction in the memory consists of a third group prefix followed by an op-code index representing an operation code, and an immediate index representing an immediate value; the op-code and the immediate indices are used to search a third sub-decoding table including a third sub-table and a fourth sub-table, respectively, the third sub-table being stored with the operation codes of the corresponding original instructions, the fourth sub-table being stored with the immediate values of the corresponding original instructions.

8. The architecture as claimed in claim 1, wherein the memory further comprises program codes each consisting of a fourth group prefix followed by an original instruction.

9. The architecture as claimed in claim 1, wherein the group prefix is encoded to have a fixed length.

10. The architecture as claimed in claim 1, wherein the group prefix is encoded to have a variable length in such a manner that the group prefix of a frequently used instruction is assigned with a relatively short code.